



Docket No.: 50090-265

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kiyotoshi UEDA, et al.

Serial No.: 09/766,845

Filed: January 23, 2001

Group Art Unit: 2829

Examiner: P. Patel

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR
INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT
MANUFACTURED THEREBY

AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following claim amendments and remarks are submitted in response to the office action dated April 11, 2003. The claims are presented in the revised claim format described in the Pre-OG notice dated January 31, 2003 regarding a waiver of the current provisions under 37 C.F.R. §§ 1.121 (a)-(d).

#11/B
7-8-03
J. Carter

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